may be employed in manufacturing a variety of different devices, e.g., memory devices, logic devices, ASICs, etc. Of course, the inventions disclosed herein should not be considered limited to the illustrative examples depicted and described herein.

As will be recognized by those skilled in the art after a complete reading of the present application, the illustrative integrated circuit product **100** described herein may be comprised of either N-type FinFET devices, P-type FinFET devices or both types of devices (CMOS application). The product **100** will be formed in and above an illustrative semiconductor substrate **120**. In this illustrative embodiment, the substrate **120** has a bulk semiconducting material configuration. The substrate **120** may be made of silicon or it may be made of materials other than silicon. Thus, the terms "substrate" or "semiconducting substrate" should be understood to cover all forms of all semiconductor materials.

In general, the methods will be disclosed in the context of forming different types of devices, e.g., logic devices, different types of SRAM devices (e.g., SRAM 1-1-1, SRAM 1-2-2) in different regions of the substrate **120**. An SRAM 1-1-1 device includes one NFET transistor that acts as a pull-down transistor, one PFET transistor that acts as a pull-up transistor and one NFET device that functions as a pass-gate transistor. An SRAM 1-2-2 device includes one PFET transistor that acts as a pull-down transistor, two NFET transistors that act as pull-up transistors and two NFET devices that function as pass-gate transistors. Accordingly, FIG. **2**A depicts a first region **110**, a second region **112** and a third region **114** of the substrate **120** at an early stage of manufacturing after various deposition processes and patterning processes have been performed. Each of the regions **110**, **112**, **114** is a contiguous part of the same substrate **120**. The regions **110**, **112**, **114** may be positioned adjacent one another or they may be spaced apart from one another on the substrate **120**, and the regions **110**, **112**, **114** may vary in physical size, and the number of devices formed in each region may also vary. As noted above, each of the regions **110**, **112**, **114** may have different types of devices formed therein. For example, the first region **110** of the substrate **120** may be used to form FinFET devices for logic circuits, the second region **112** may be used to form FinFET devices for a first type of SRAM devices, and the third region **114** may be used to form FinFET devices for a second type of SRAM devices. Of course, the devices that are formed in each of the regions may vary depending upon the application.

With continuing reference to FIG. **2**A, several process operations have been performed on the integrated circuit product **100**. First, a pad layer **122**, a lower hard mask layer **124**, a lower mandrel layer **126**, an upper hard mask layer **128** and an upper mandrel layer **130** were sequentially formed above the substrate **120**. Thereafter various material layers **132**, **134** and **136** that will collectively be used to form or be part of a patterned mask layer **129** above the first region **110** were formed above the upper mandrel layer **130**. In one embodiment, the layer **132** may be an OPL layer, the layer **134** may be an anti-reflective coating (ARC) layer and the layer **136** may be a photoresist material. FIG. **2**A depicts the product **100** after the photoresist layer **136** and the ARC layer **134** were initially patterned above only the first region **110** using traditional photolithography techniques, and after an etching process was performed through the patterned layers **136**, **134** so as to thereby define the patterned masking layer **129** comprised of features **131**, that includes the patterned OPL layer **132**A. This etching process stops on the upper mandrel layer **130** in the first region **110**. The features **131** (i.e., the remaining regions **132**A, **134**A, **136**A) of the patterned masking layer **129** have a lateral width **133** and a pitch **135** (not illustrated to scale). In at least one illustrative embodiment, the width **133** may be approximately 40 nm and the pitch **135** may be approximately 120 nm. Of course, the width and pitch dimensions may vary depending upon the application.

The layers of material depicted in FIG. **2**A may be made of various materials depending upon the particular application. For example, in at least one illustrative embodiment, the pad layer **122** may be made of silicon dioxide, the hard mask layers **124**, **128** may be made of silicon nitride and the mandrel layers **126**, **130** may be made of amorphous silicon. The ARC layer **124** may be made of a variety of materials in various embodiments, such as silicon nitride, silicon oxynitride, silicon or carbon-containing organic polymers, etc., depending upon the application. The various layers shown in FIG. **2**A may be deposited in various thicknesses depending upon the application. For example, in at least one illustrative embodiment, the hard mask layers **124**, **128** may each be about 30 nm thick, the mandrel layers **126**, **130** may each be about 100 nm thick, the OPL layer **132** may be about 100 nm thick and the ARC layer may be about 35 nm thick. The layers of material depicted in FIG. **2**A may be formed by performing any of a variety of known processing techniques, e.g., chemical vapor deposition (CVD), atomic layer deposition (ALD), physical vapor deposition (PVD), spin-coating, etc.

FIG. **2**B depicts the product **100** after several process operations were performed. First, in one embodiment, the layers **136** and **134** may be removed leaving only the patterned OPL layer **132** as the patterned masking layer **129**. In other cases, the layers **136** and **134** may remain as part of the patterned masking layer **129**. Irrespective of the number of layers of material in the patterned masking layer **129**, FIG. **2**B depicts the product **100** after one or more anisotropic etching processes were performed through the patterned masking layer **129** to pattern the upper mandrel layer **130** relative to the surrounding materials and define a patterned upper mandrel layer **130**X comprised of upper mandrel structures or features **130**A above the first region **110** only of the product **100**. At least the remaining portions of the OPL layer **132** positioned above the second and third regions **112**, **114** protect the upper mandrel layer **130** above the second **112** and third **114** regions of the substrate **120** from the etching processes. In at least one illustrative embodiment, features of the upper mandrel structures **130**A have a lateral width **137** and a pitch **139**, which may be approximately 40 nm and 120 nm respectively. After the patterned upper mandrel layer **130**X is formed only above the first region **110**, the materials positioned above the upper mandrel layer **130** and the patterned upper mandrel layer **130**X are removed from all three regions **110**, **112** and **114** of the substrate **120**.

FIG. **2**C depicts the product **100** after a layer of spacer material **140** was deposited above the substrate **120**. In at least one illustrative embodiment, the layer of spacer material **140** may be approximately 20 nm thick and it may be made of silicon dioxide. The thickness and material of the layer of spacer material **140** may vary depending upon the application.

FIG. **2**D depicts the product **100** after an anisotropic etching process was performed on the layer of spacer material **140** above all three regions **110**, **112**, **114** of the substrate **120** to remove horizontally positioned portions of the layer of spacer material **140**. This results in the formation